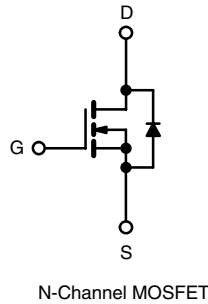
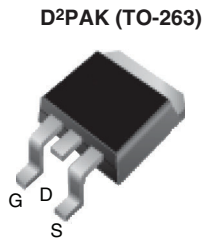


## Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	500
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$ 0.52
$Q_g$ (Max.) (nC)	52
$Q_{gs}$ (nC)	13
$Q_{gd}$ (nC)	18
Configuration	Single



### FEATURES

- Low Gate Charge  $Q_g$  results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective  $C_{OSS}$  Specified
- Lead (Pb)-free Available



Available  
**RoHS\***  
COMPLIANT

### APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching

### TYPICAL SMPS TOPOLOGIES

- Two Transistor Forward
- Half and Full Bridge
- Power Factor Correction Boost

ORDERING INFORMATION			
Package	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)
Lead (Pb)-free	IRFS11N50APbF	IRFS11N50ATRRPbF <sup>a</sup>	IRFS11N50ATRLPbF <sup>a</sup>
	SiHFS11N50A-E3	SiHFS11N50ATR-E3 <sup>a</sup>	SiHFS11N50ATL-E3 <sup>a</sup>
SnPb	IRFS11N50A	-	IRFS11N50ATRL <sup>a</sup>
	SiHFS11N50A	-	SiHFS11N50ATL <sup>a</sup>

#### Note

a. See device orientation.


ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted					
PARAMETER			SYMBOL	LIMIT	UNIT
Gate-Source Voltage			$V_{GS}$	$\pm 30$	V
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	$I_D$	11	A
		$T_C = 100\text{ }^\circ\text{C}$		7.0	
Pulsed Drain Current <sup>a</sup>			$I_{DM}$	44	
Linear Derating Factor				1.3	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy <sup>b</sup>			$E_{AS}$	275	mJ
Repetitive Avalanche Current <sup>a</sup>			$I_{AR}$	11	A
Repetitive Avalanche Energy <sup>a</sup>			$E_{AR}$	17	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$		$P_D$	170	W
Peak Diode Recovery $dV/dt^c$			$dV/dt$	6.9	V/ns
Operating Junction and Storage Temperature Range			$T_J, T_{stg}$	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s			300 <sup>d</sup>	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 19\text{ mH}$ ,  $R_G = 25\text{ }^\circ\Omega$ ,  $I_{AS} = 5.5\text{ A}$  (see fig. 12).
- $I_{SD} \leq 5.5\text{ A}$ ,  $dI/dt \leq 90\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

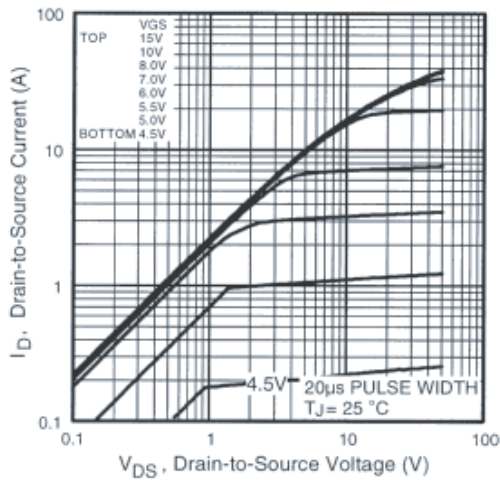
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.75	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.50	-	
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	500	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$	-	0.060	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	$\mu\text{A}$
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 6.6\text{ A}^b$	-	-	0.52	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 6.6\text{ A}$	6.1	-	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}, \text{ see fig. 5}$	-	1423	-	pF
Output Capacitance	$C_{oss}$		-	208	-	
Reverse Transfer Capacitance	$C_{rss}$		-	8.1	-	
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	2000	
Effective Output Capacitance	$C_{oss\text{ eff.}}$		$V_{DS} = 400\text{ V}, f = 1.0\text{ MHz}$	-	55	-
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}, I_D = 11\text{ A}, V_{DS} = 400\text{ V}$ see fig. 6 and 13 <sup>b</sup>	-	-	52	nC
Gate-Source Charge	$Q_{gs}$		-	-	13	
Gate-Drain Charge	$Q_{gd}$		-	-	18	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250\text{ V}, I_D = 11\text{ A}, R_G = 9.1\text{ }\Omega, R_D = 22\text{ }\Omega,$ see fig. 10 <sup>b</sup>	-	14	-	ns
Rise Time	$t_r$		-	35	-	
Turn-Off Delay Time	$t_{d(off)}$		-	32	-	
Fall Time	$t_f$		-	28	-	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	11	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	44	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 11\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 11\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$	-	510	770	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	3.4	5.1	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

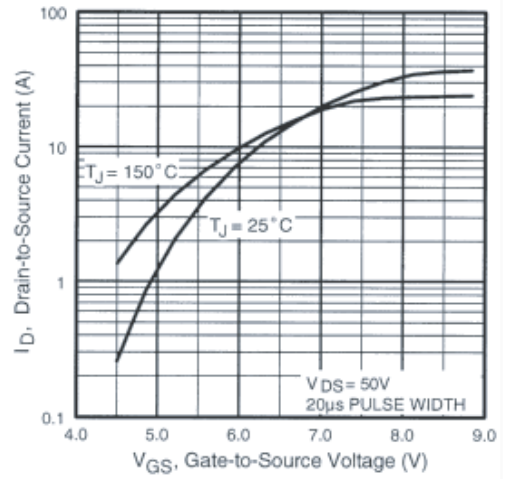
### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DS}$ .

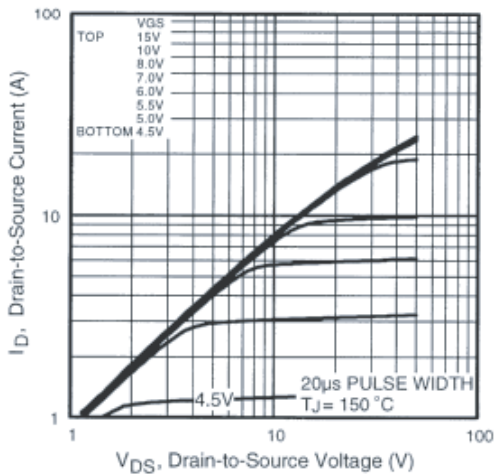
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



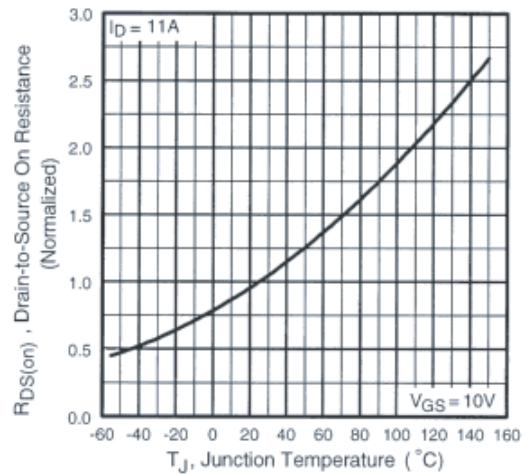
**Fig. 1 - Typical Output Characteristics**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 2 - Typical Output Characteristics**



**Fig. 4 - Normalized On-Resistance vs. Temperature**

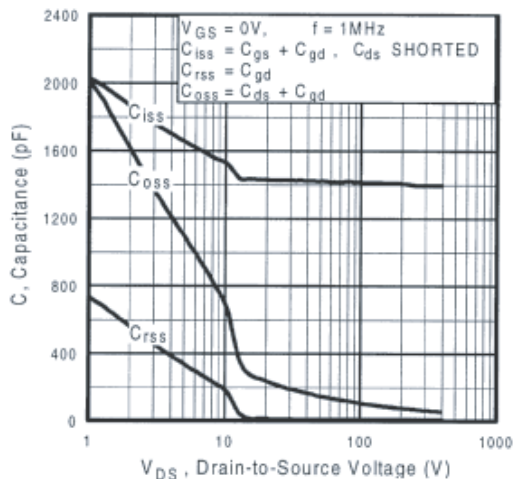


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

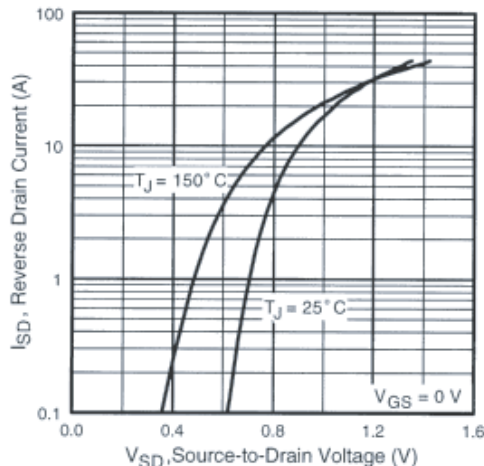


Fig. 7 - Typical Source-Drain Diode Forward Voltage

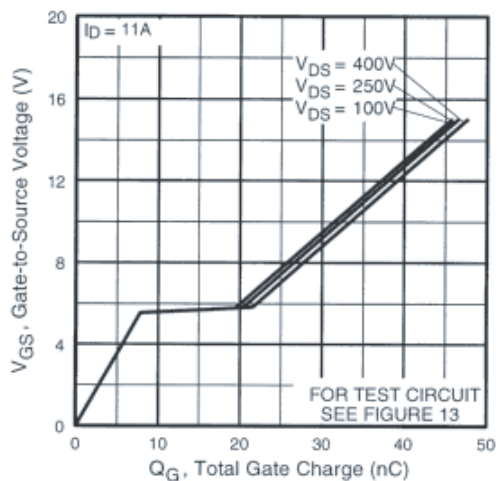


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

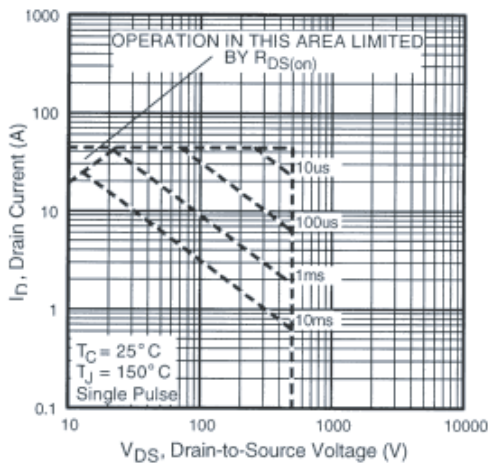


Fig. 8 - Maximum Safe Operating Area

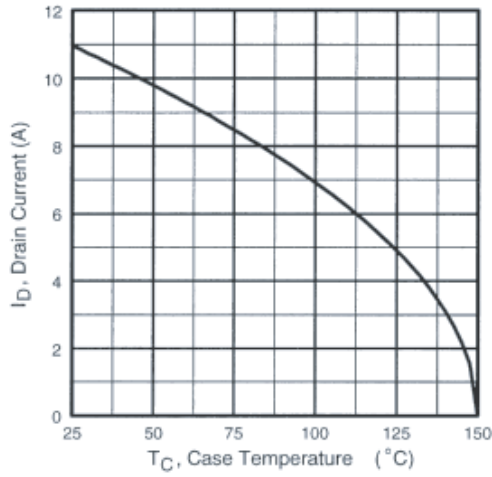


Fig. 9 - Maximum Drain Current vs. Case Temperature

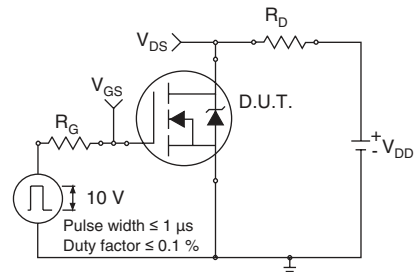


Fig. 10a - Switching Time Test Circuit

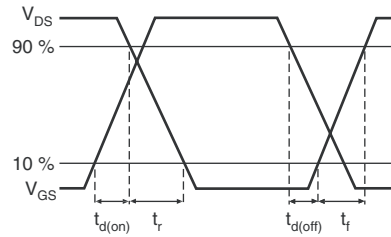


Fig. 10b - Switching Time Waveforms

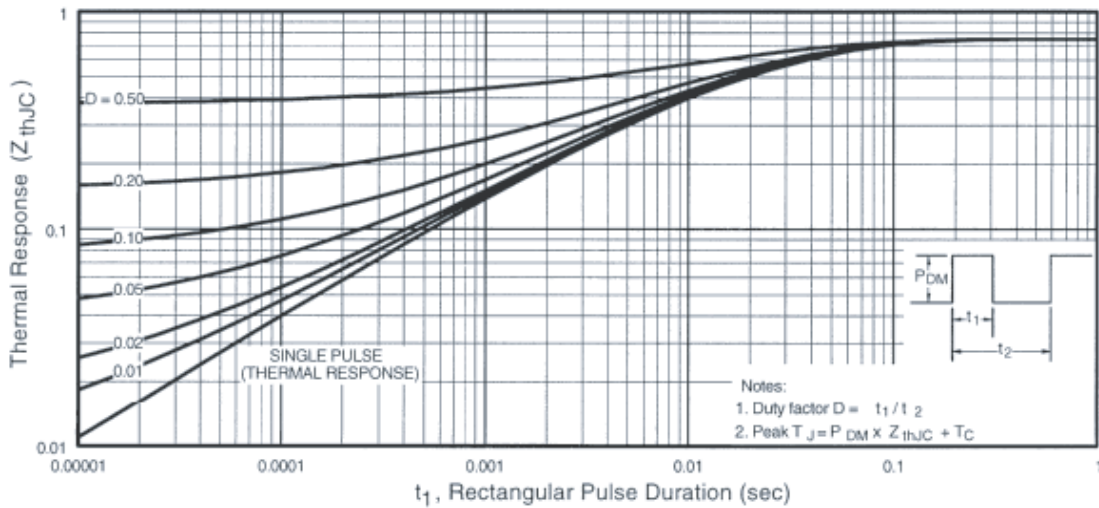


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

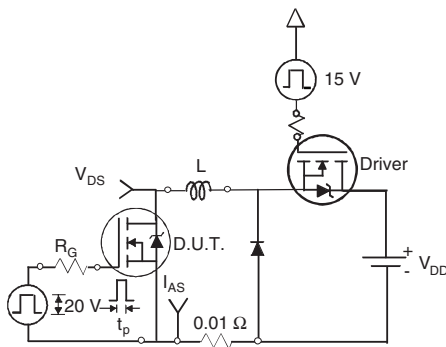


Fig. 12a - Unclamped Inductive Test Circuit

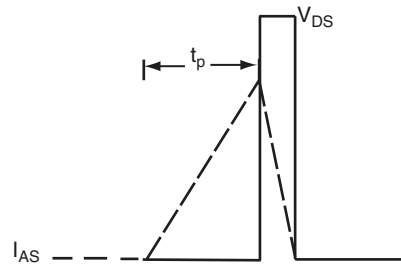


Fig. 12b - Unclamped Inductive Waveforms

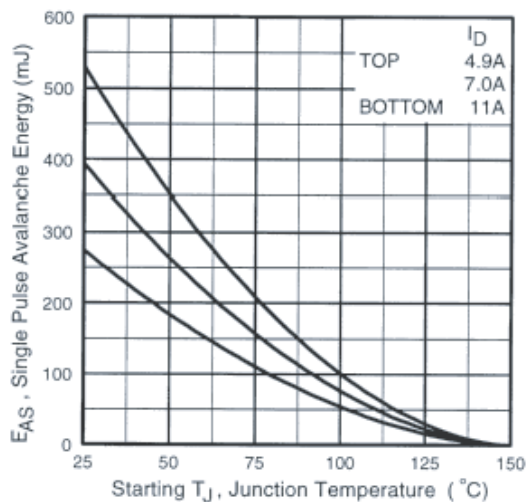


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

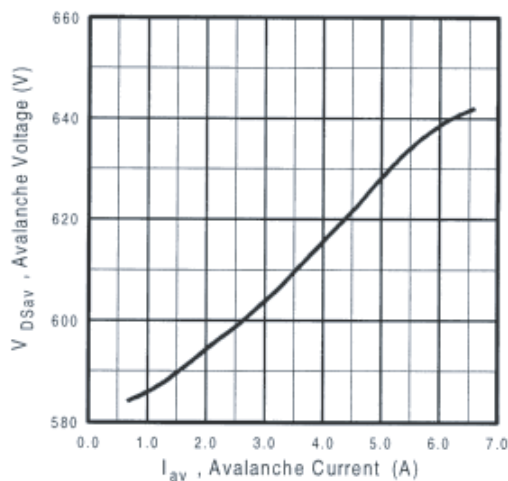


Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

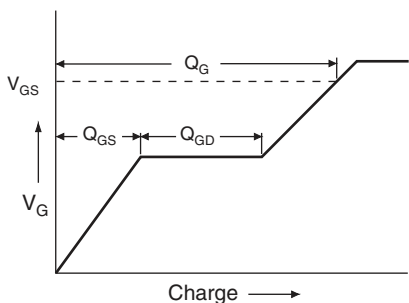


Fig. 13a - Basic Gate Charge Waveform

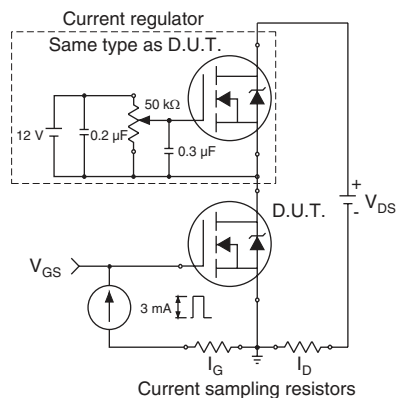
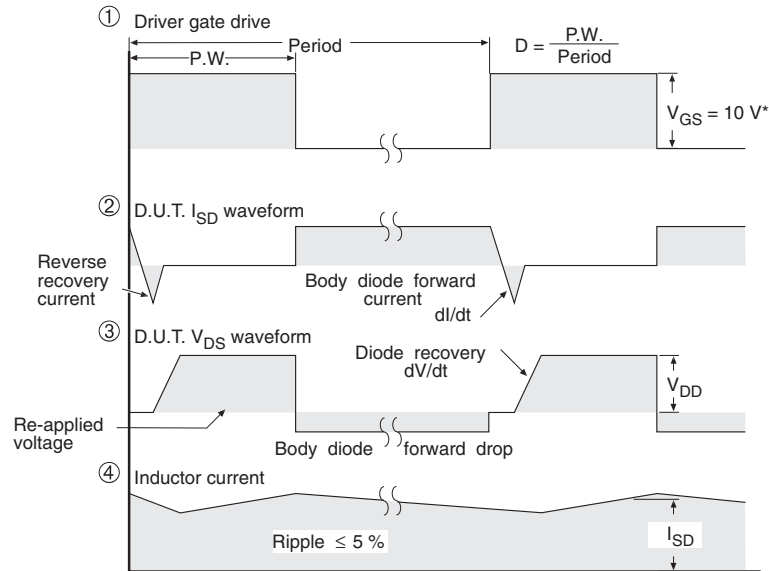
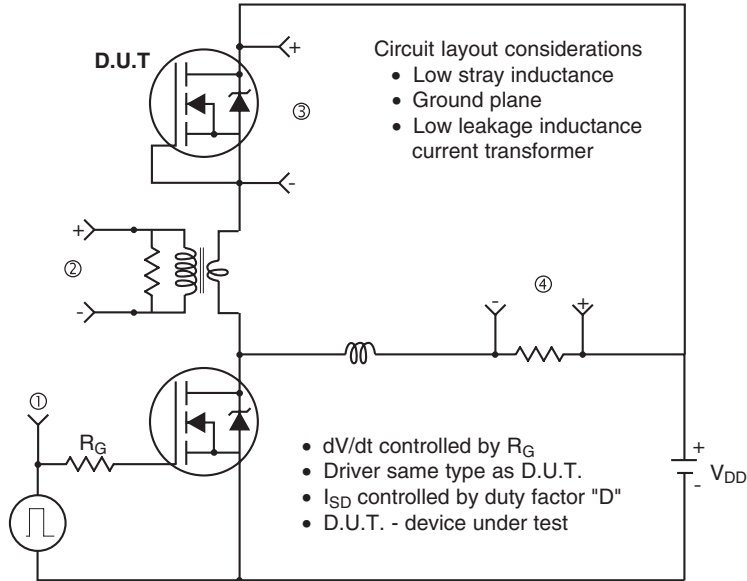


Fig. 13b - Gate Charge Test Circuit

## Peak Diode Recovery dV/dt Test Circuit



\*  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

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